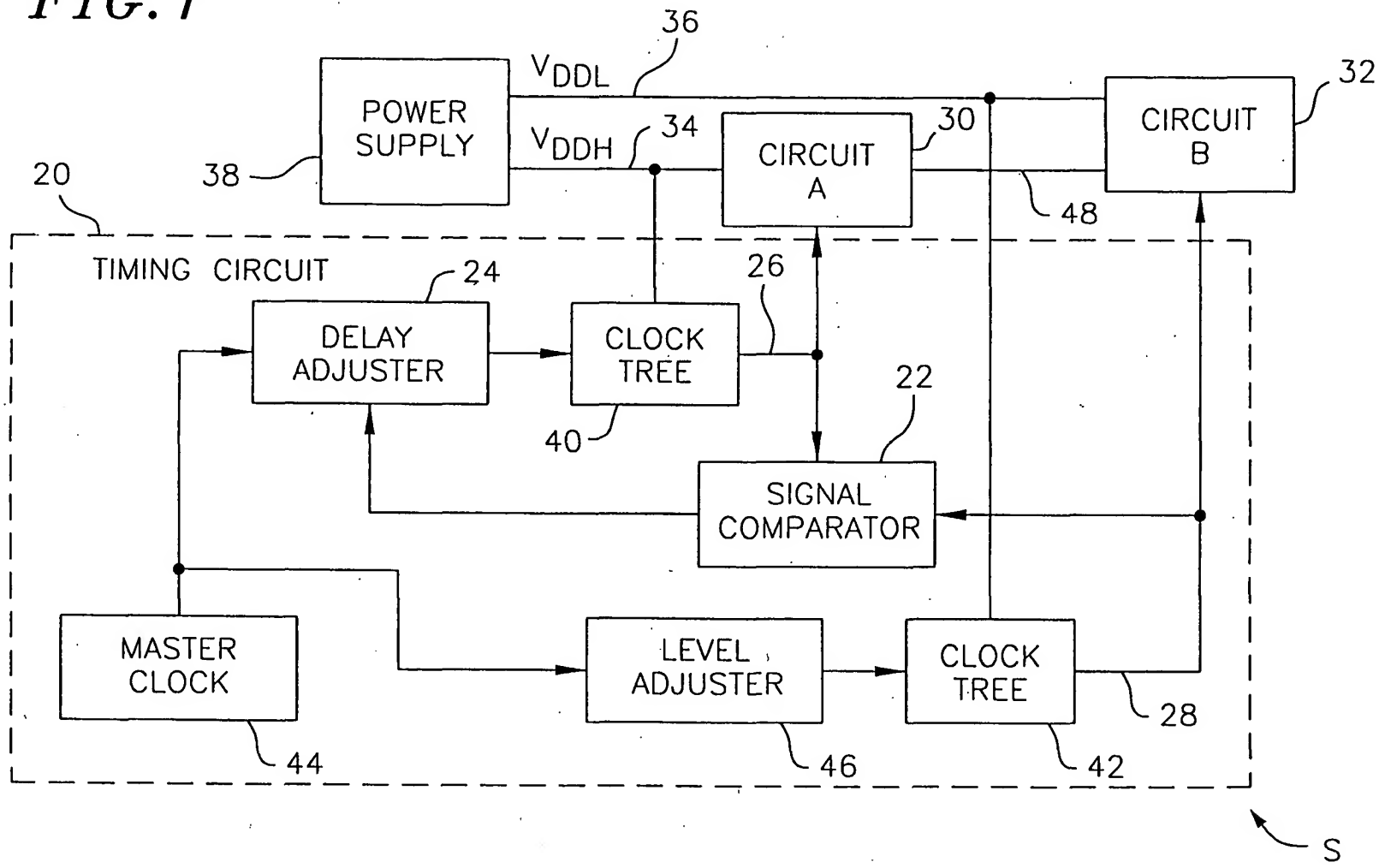
FIG. 1


36
V_{DDL}
POWER SUPPLY
V_{DDH}
34
38
20
CIRCUIT A
30
CIRCUIT B
32
48
TIMING CIRCUIT
24
DELAY ADJUSTER
CLOCK TREE
26
40
22
SIGNAL COMPARATOR
MASTER CLOCK
LEVEL ADJUSTER
CLOCK TREE
28
44
46
42
S

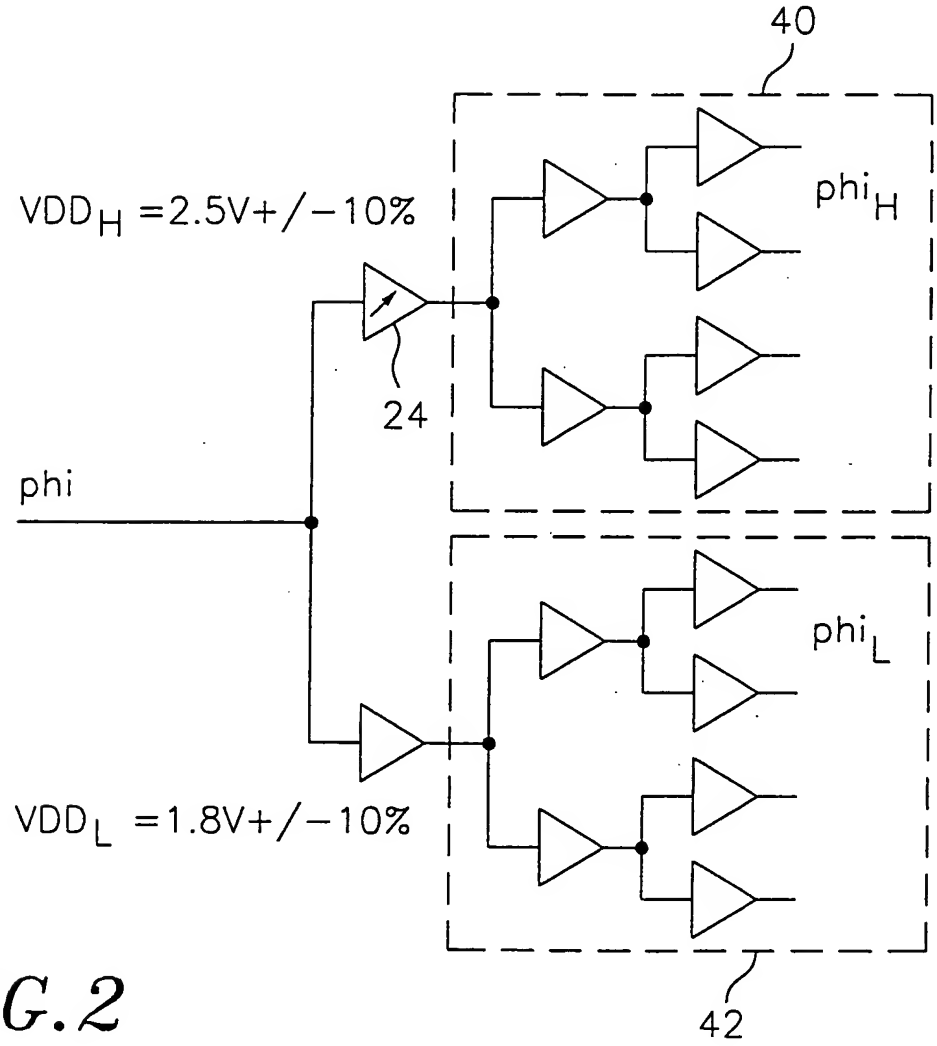
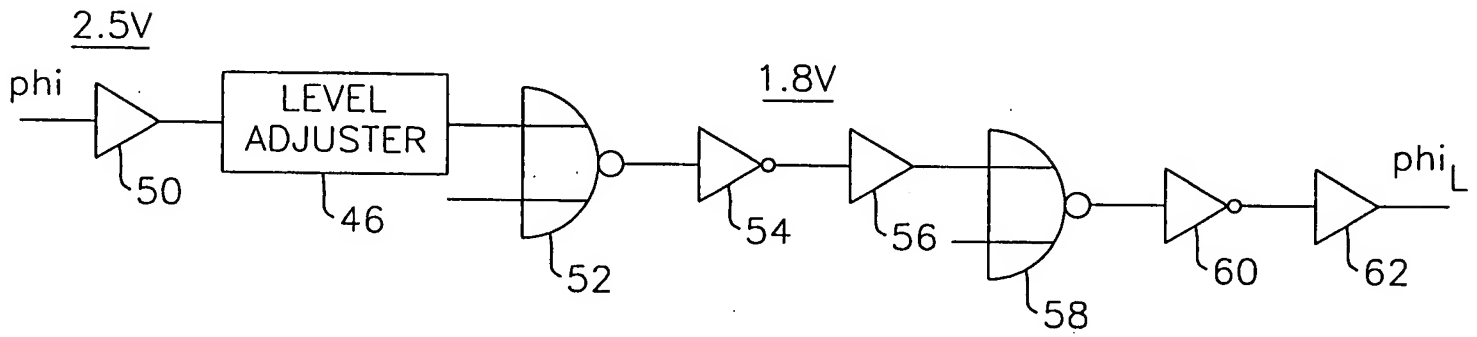


FIG.2



DELAY/ns				Σ
SS	0.42	1.78	1.25	3.45
TT	0.26	1.02	0.72	2.00
FF	0.20	0.68	0.48	1.36

FIG.3

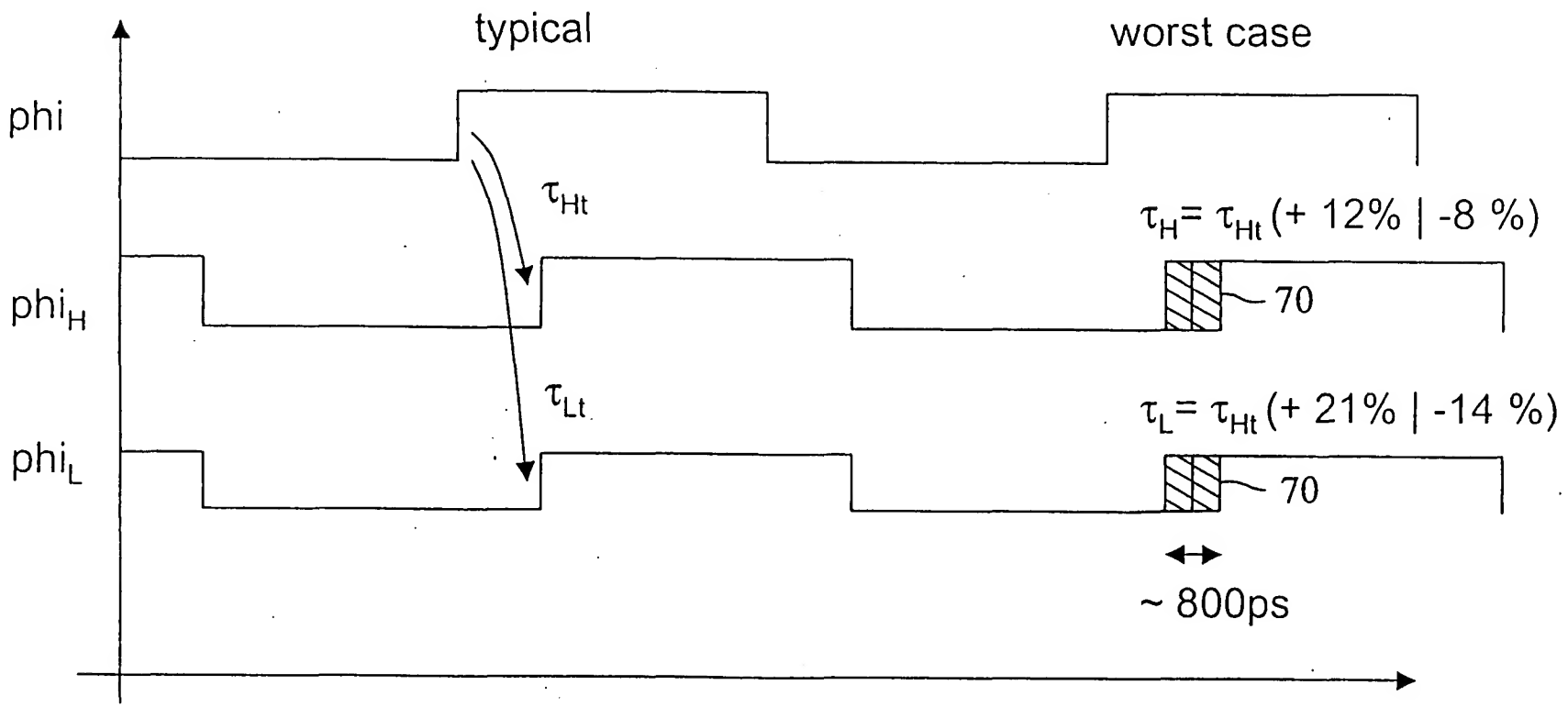

typical
worst case
phi
τ_{Ht}
$\tau_H = \tau_{Ht}$ (+ 12% | -8 %)
phi_H
70
τ_{Lt}
$\tau_L = \tau_{Ht}$ (+ 21% | -14 %)
phi_L
70
~ 800ps

FIG. 4

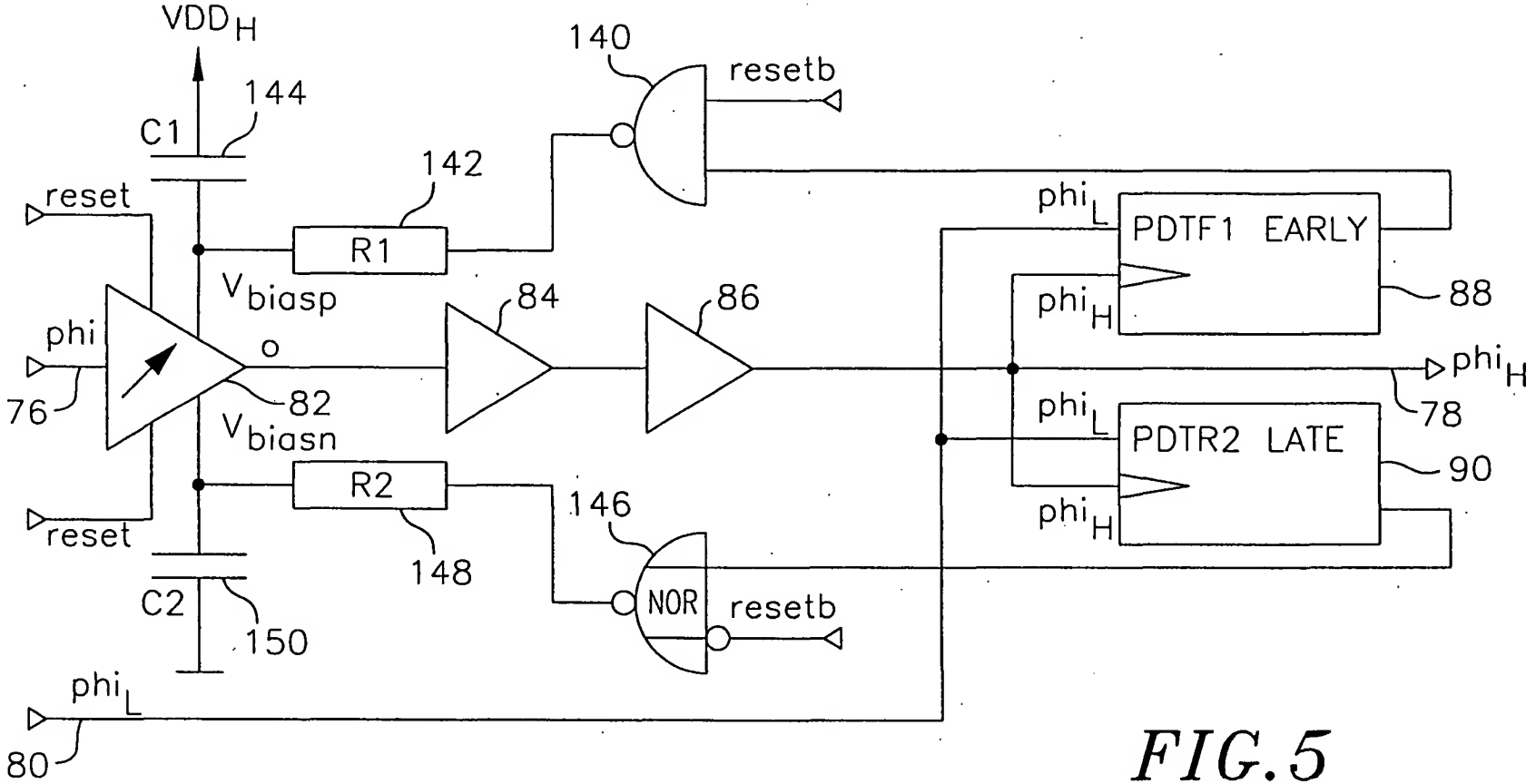
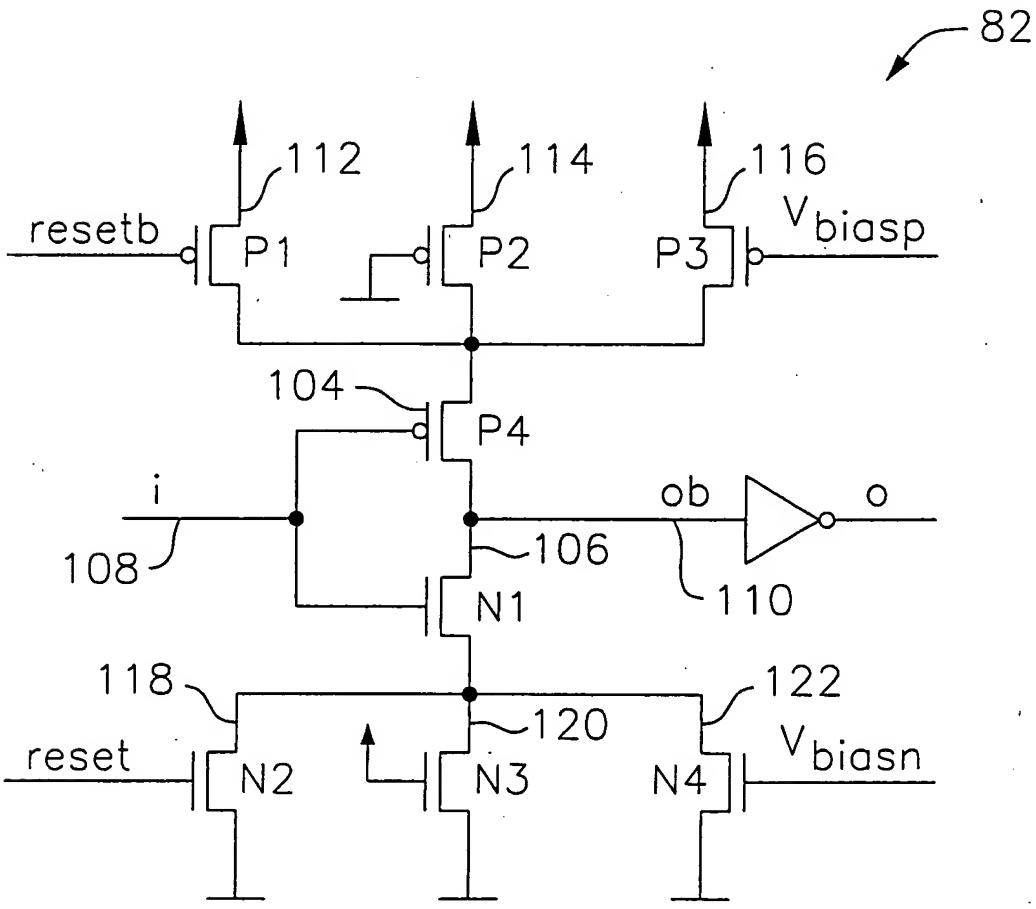
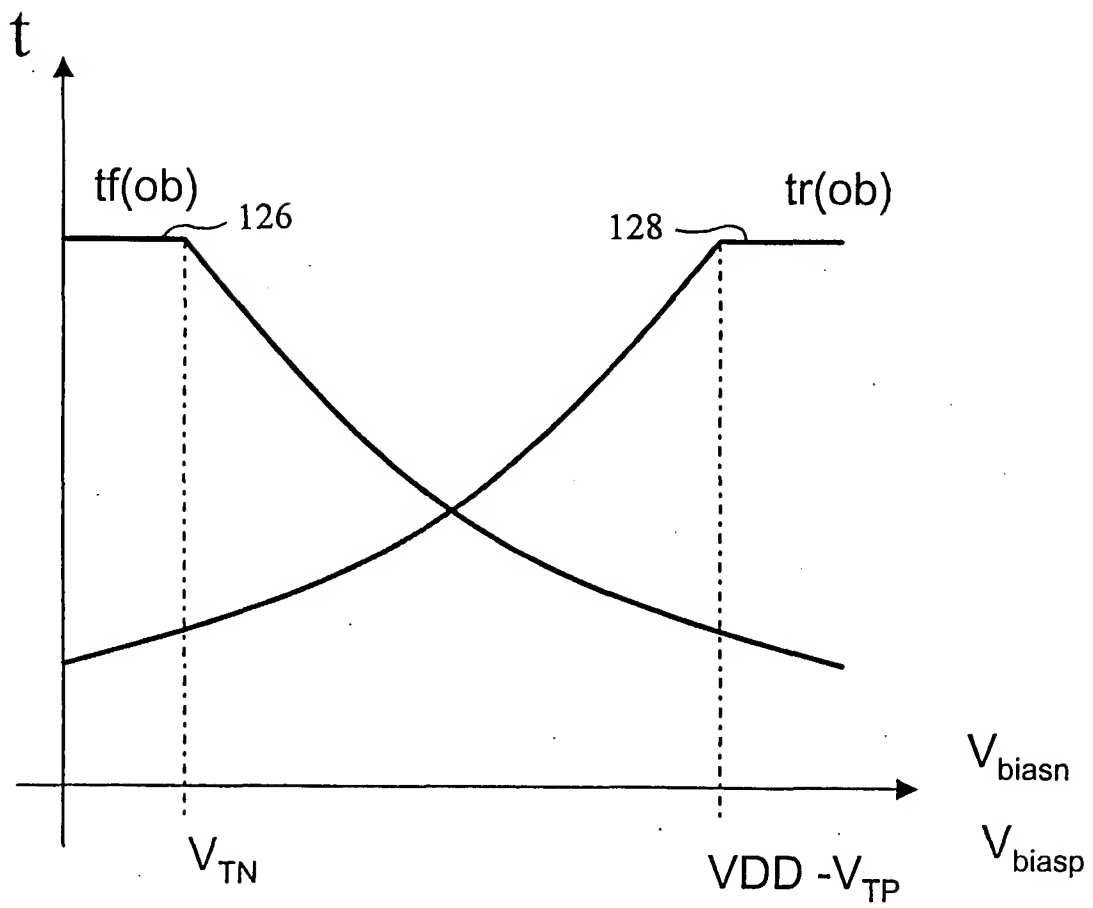

VDD H
144
C1
reset
142
R1
140
resetb
phi L
PDTF1 EARLY
phi H
88
Vbiasp
phi
o
84
86
phi H
76
82
78
Vbiasn
phi L
PDTR2 LATE
R2
90
146
phi H
reset
148
C2
NOR
resetb
150
phi L
80

FIG. 5

FIG.6


82
112
114
116
resetb
P1
P2
P3
V_{biasp}
104
P4
i
ob
o
108
106
110
N1
118
122
120
reset
N2
N3
N4
V_{biasn}



tr: rise time
tf: fall time

FIG. 7

FIG. 8A

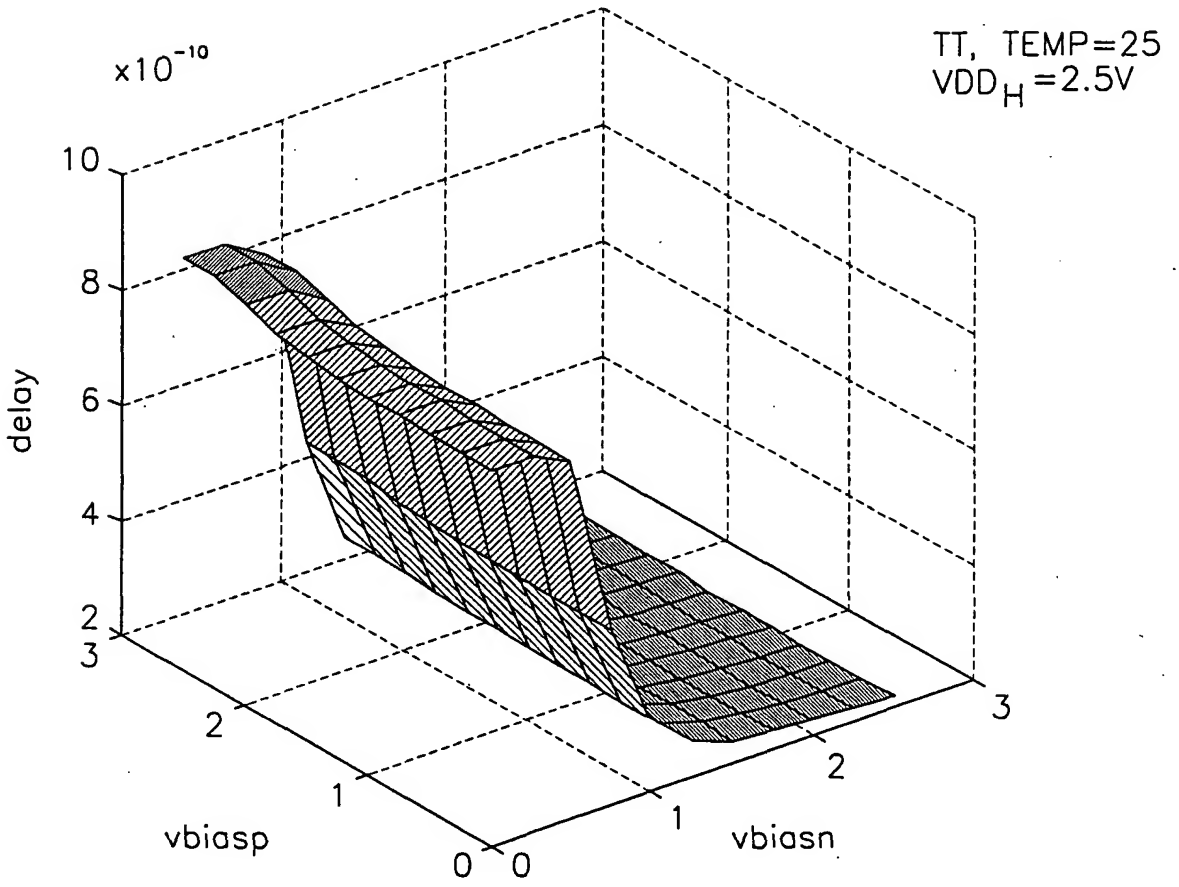

delays, CORNER=2, 01phi>01phi1
TT, TEMP=25
VDD_H=2.5V
x10^-10
10
8
6
4
2
delay
3
2
1
0
vbiasp
0
1
2
3
vbiasn

FIG.8B

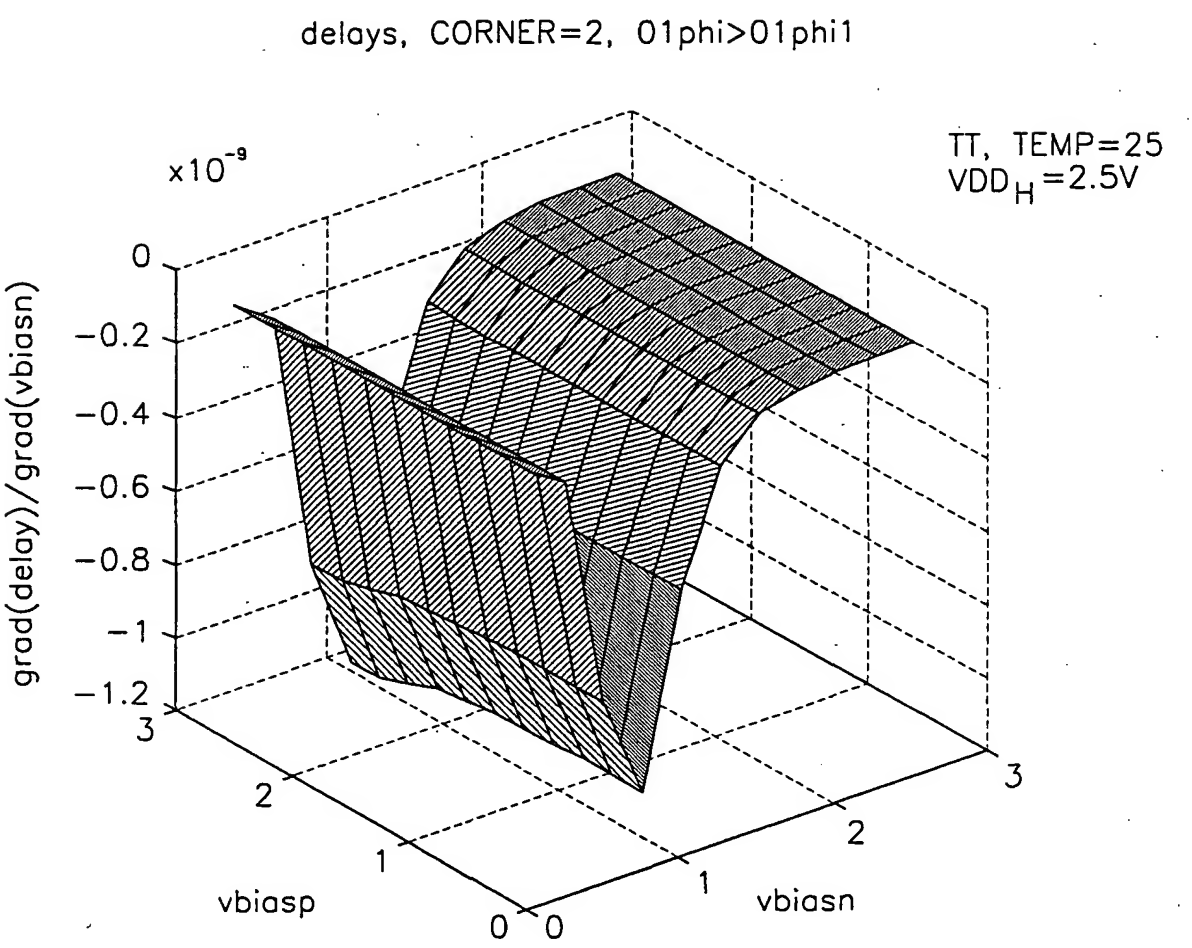

delays, CORNER=2, 01phi>01phi1
TT, TEMP=25
VDD_H=2.5V
x10^-9
grad(delay)/grad(vbiasn)
0
−0.2
−0.4
−0.6
−0.8
−1
−1.2
vbiasp
vbiasn
0
1
2
3

FIG.8C

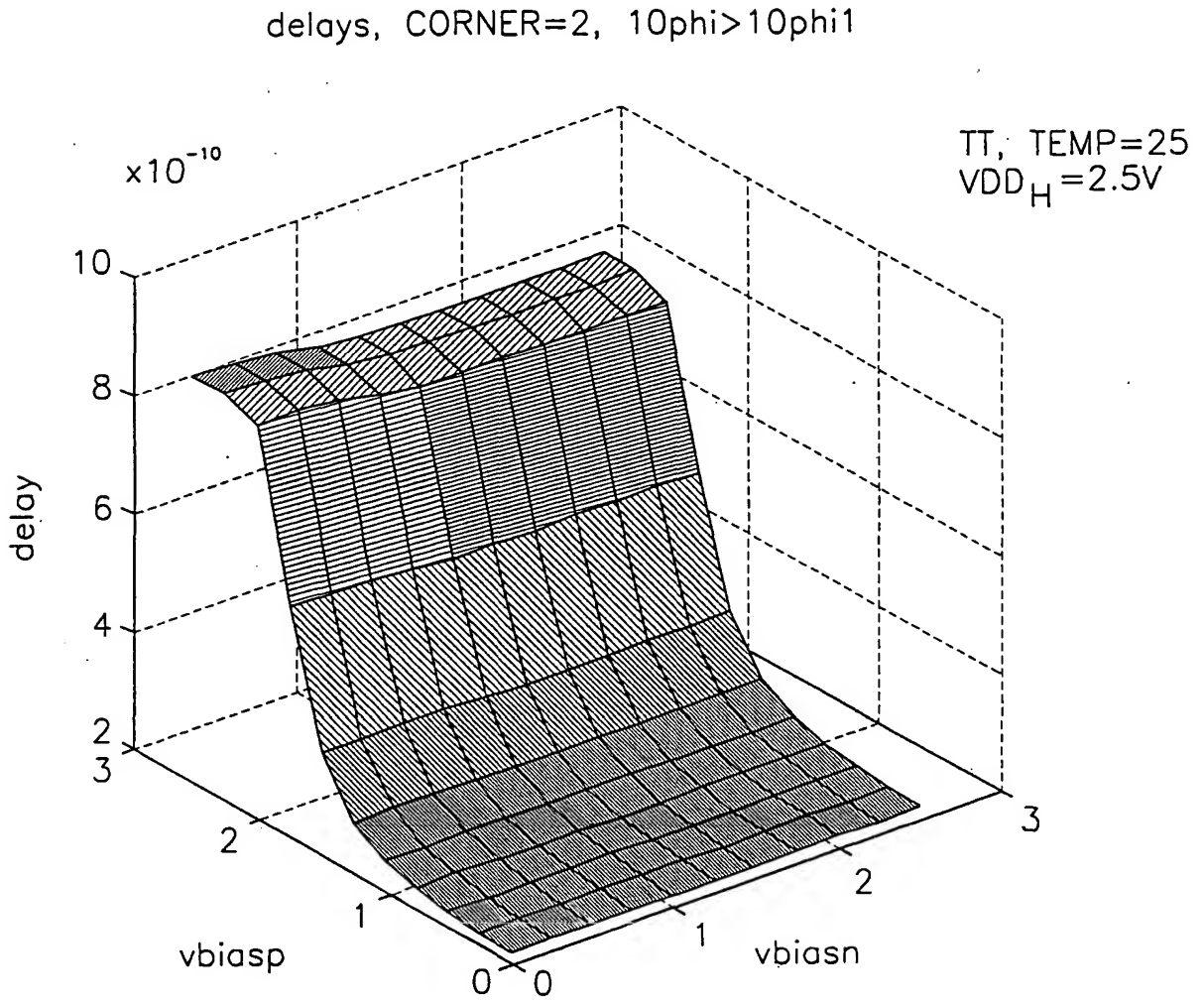

delays, CORNER=2, 10phi>10phi1
TT, TEMP=25
VDD H =2.5V
x10^-10
10
8
6
4
2
delay
3
2
1
0
vbiasp
0
1
2
3
vbiasn

FIG.8D

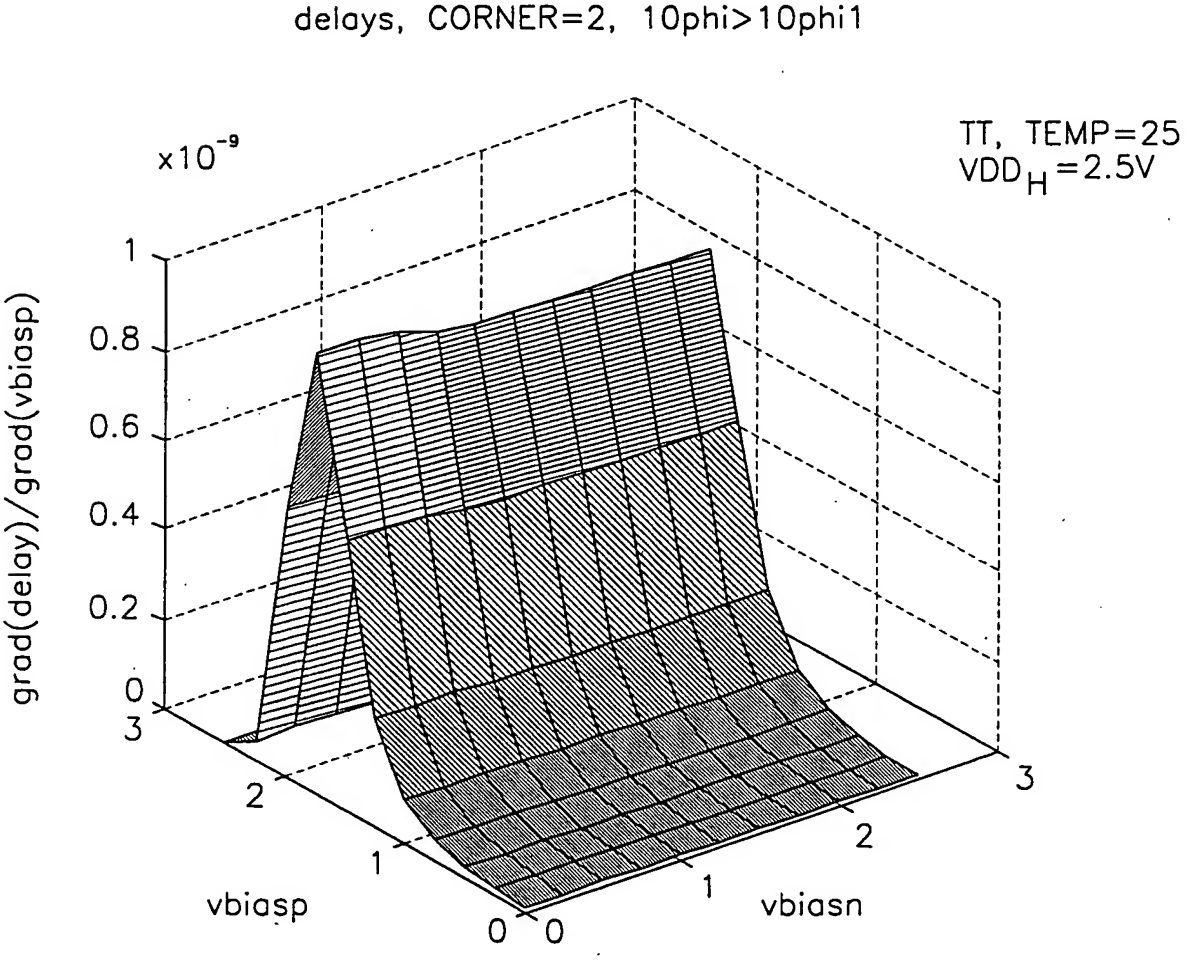

delays, CORNER=2, 10phi>10phi1
TT, TEMP=25
VDD H =2.5V
x10^-9
grad(delay)/grad(vbiasp)
1
0.8
0.6
0.4
0.2
0
3
2
1
0
vbiasp
0
1
2
3
vbiasn

FIG. 9

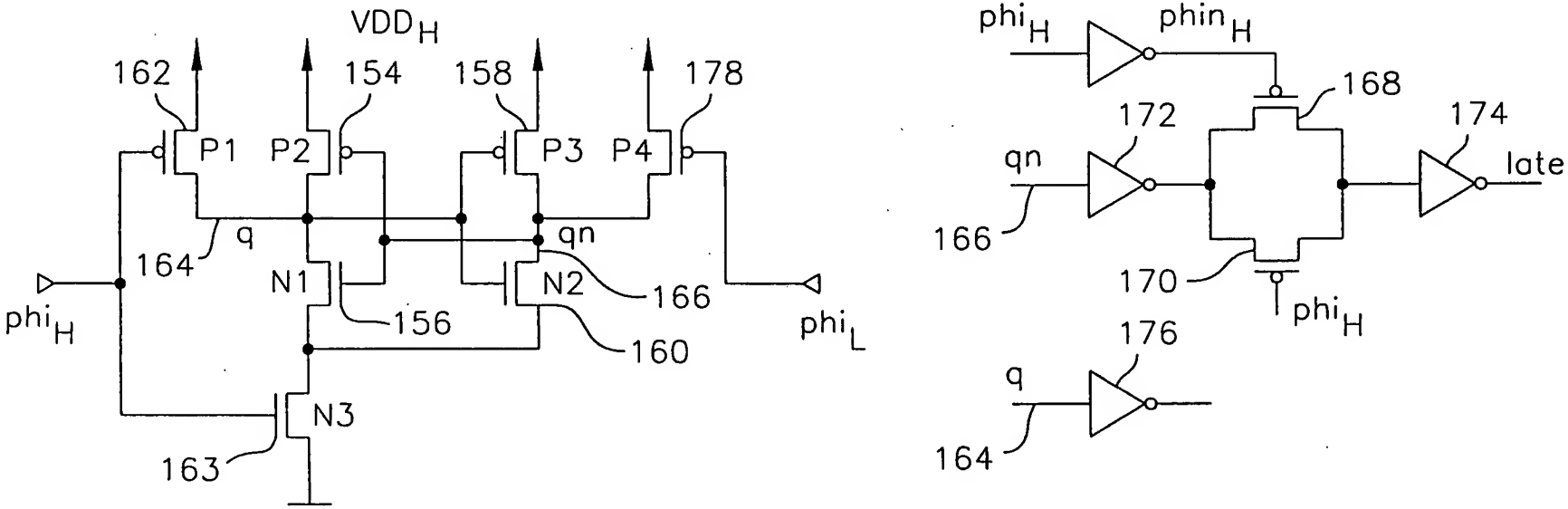
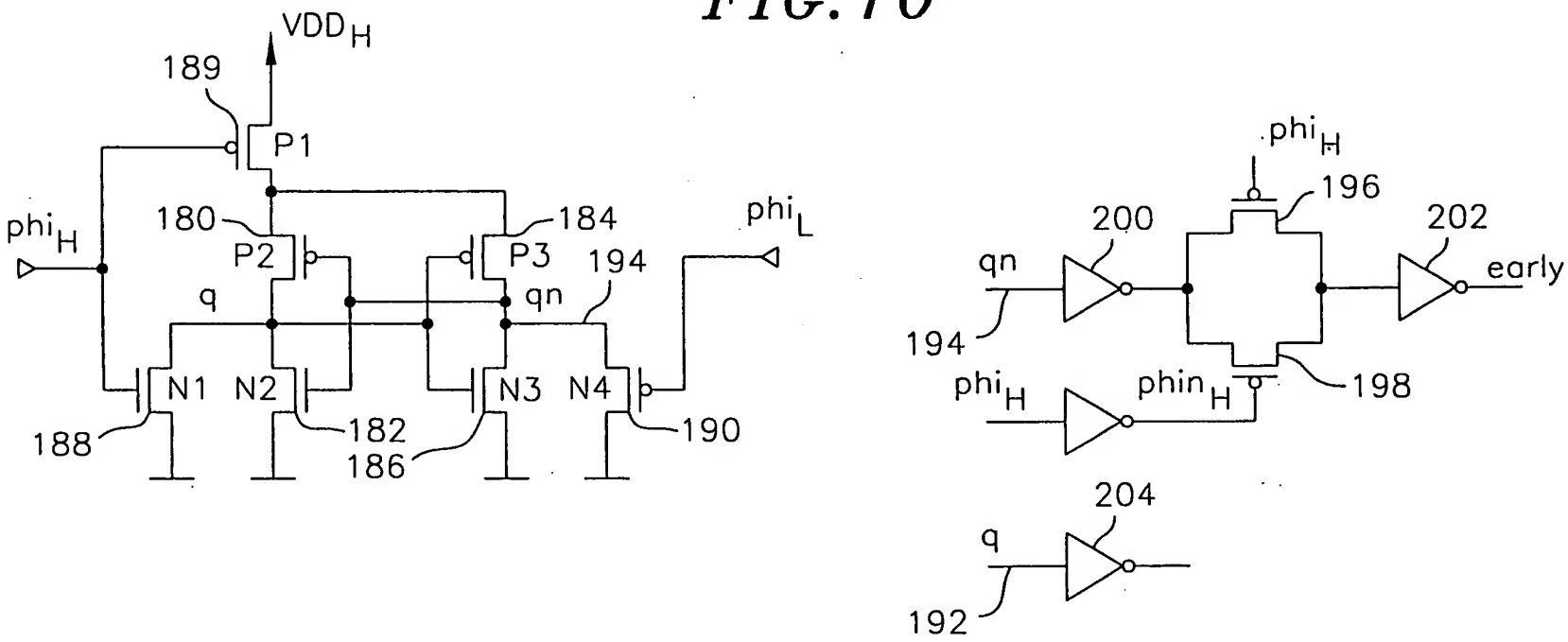

VDD_H
162
154
158
178
P1
P2
P3
P4
q
qn
164
N1
N2
166
156
160
phi_H
phi_L
N3
163
phi_H
phin_H
168
172
174
qn
late
166
170
phi_H
176
q
164

FIG. 10


VDD H
189
P1
phi H
180
P2
184
P3
phi L
194
q
qn
N1
N2
N3
N4
188
182
186
190
phi H
196
200
202
qn
early
194
phi H
phin H
198
204
q
192

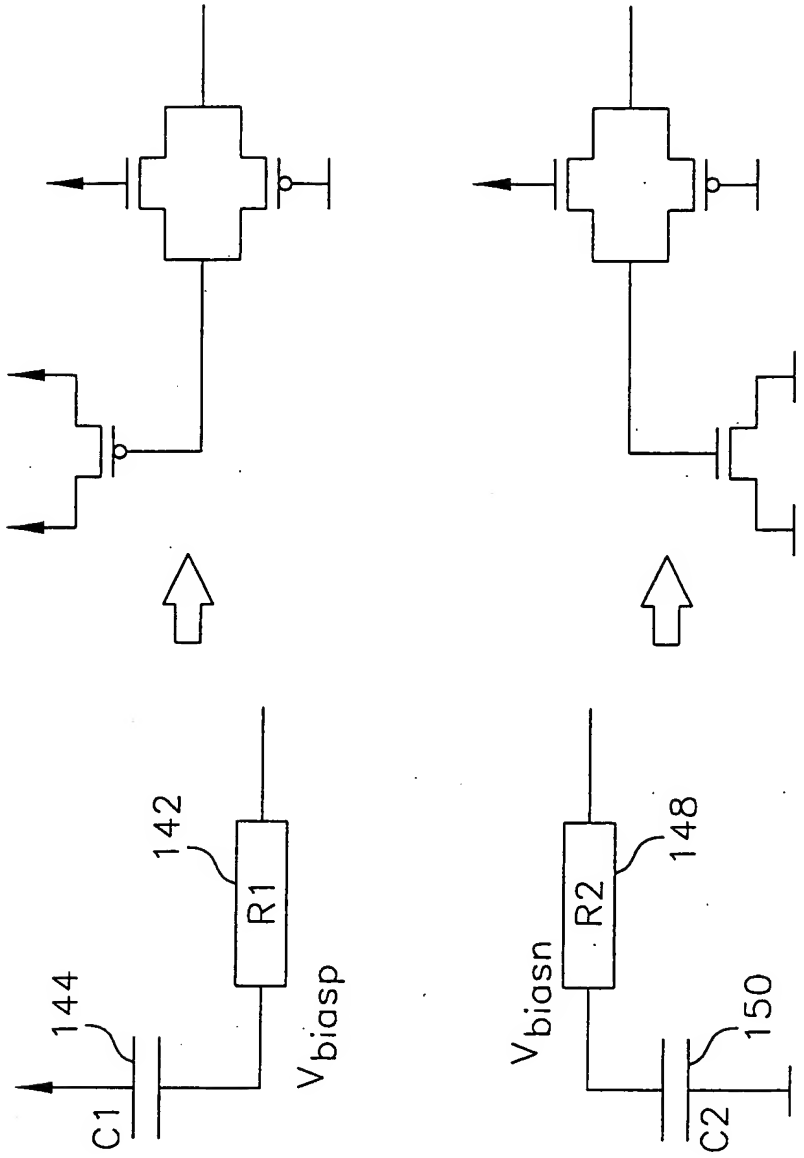


FIG. 11

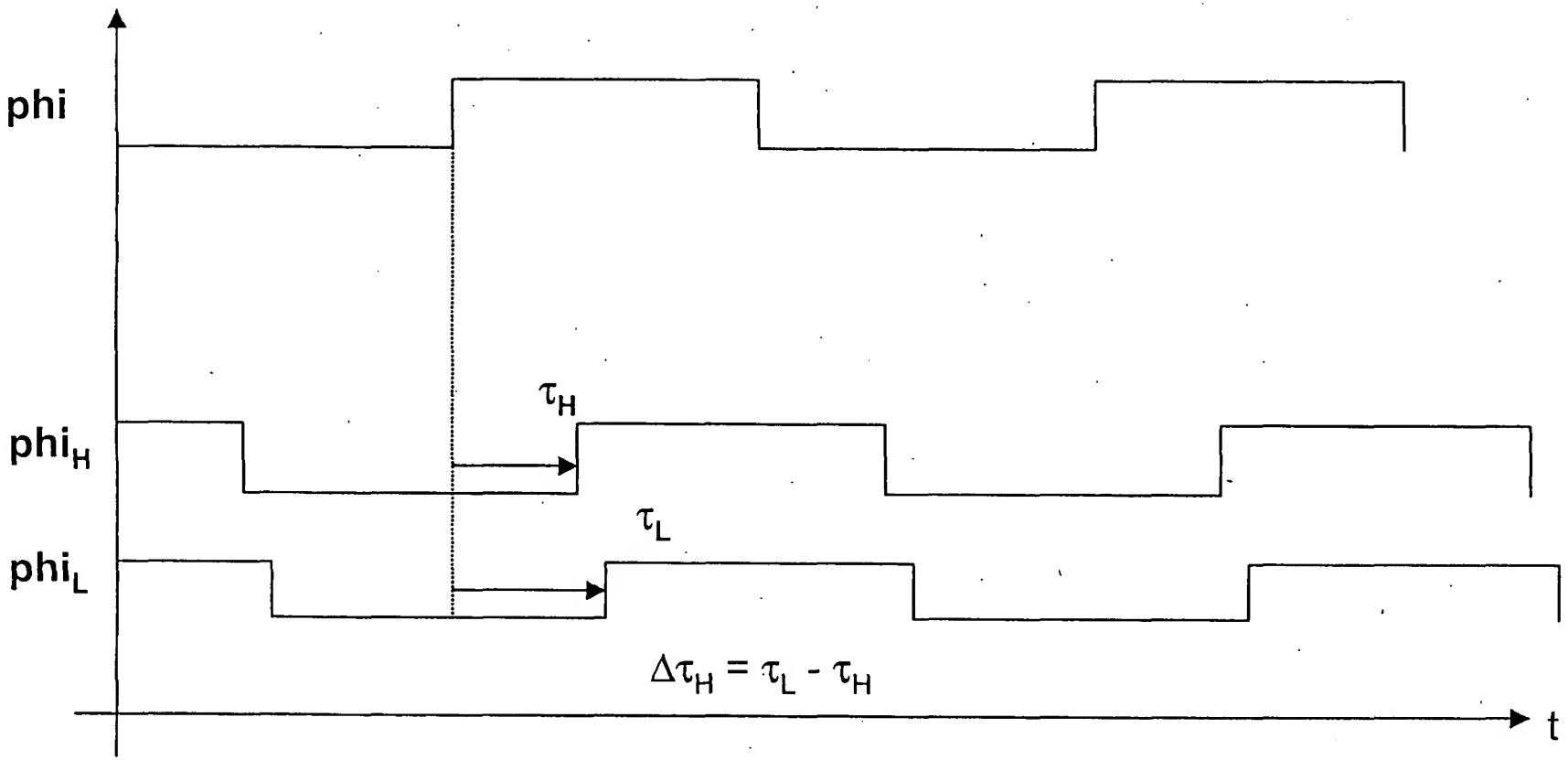


FIG. 12

FIG. 13A

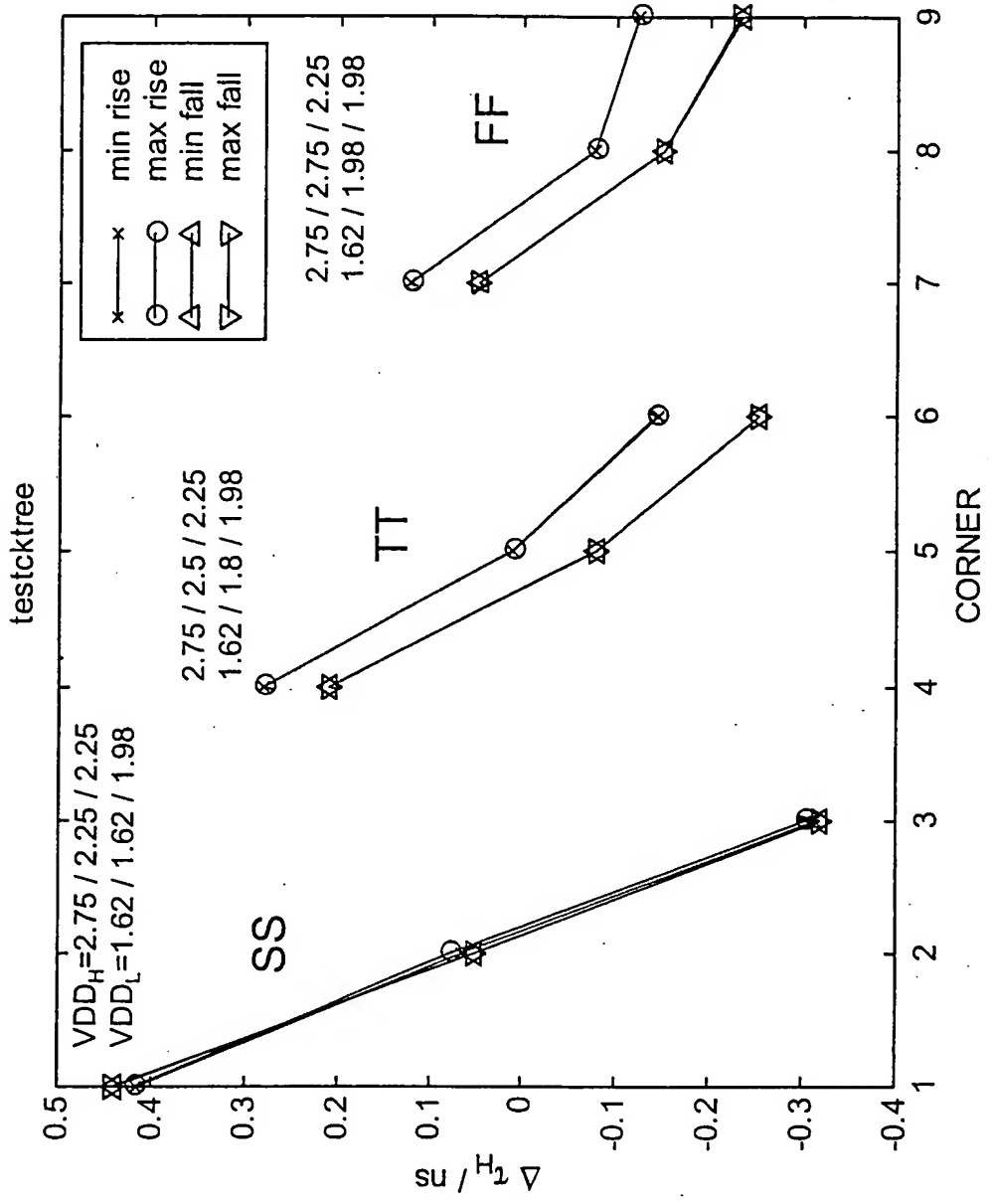

testcktree
VDD_H=2.75 / 2.25 / 2.25
VDD_L=1.62 / 1.62 / 1.98
2.75 / 2.5 / 2.25
1.62 / 1.8 / 1.98
2.75 / 2.75 / 2.25
1.62 / 1.98 / 1.98
SS
TT
FF
min rise
max rise
min fall
max fall
Δ τH / ns
CORNER
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
1
2
3
4
5
6
7
8
9

FIG. 13B

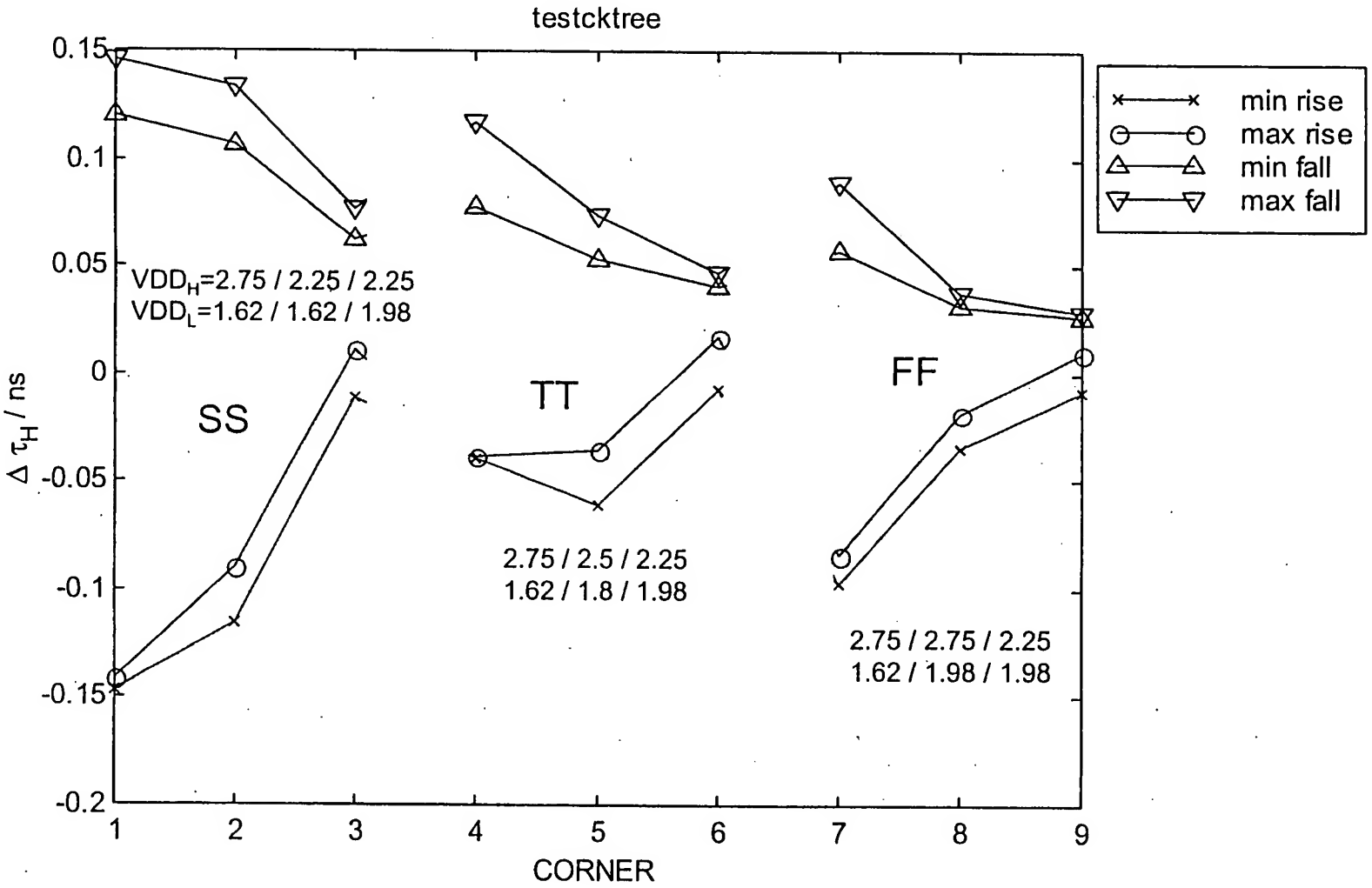

testcktree
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
1
2
3
4
5
6
7
8
9
CORNER
Δ τH / ns
min rise
max rise
min fall
max fall
VDDH=2.75 / 2.25 / 2.25
VDDL=1.62 / 1.62 / 1.98
SS
TT
FF
2.75 / 2.5 / 2.25
1.62 / 1.8 / 1.98
2.75 / 2.75 / 2.25
1.62 / 1.98 / 1.98

FIG. 13C

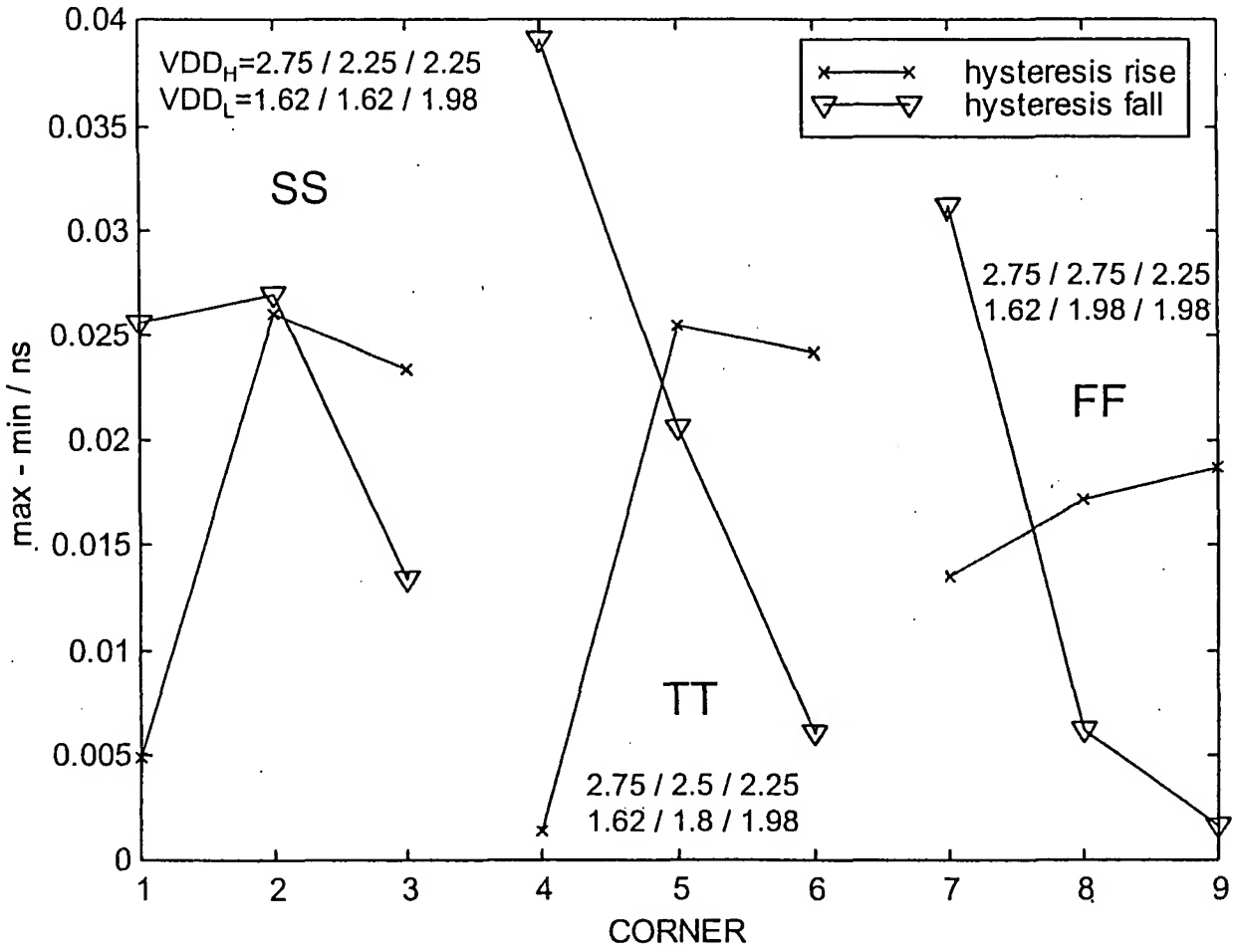

VDD$_H$=2.75 / 2.25 / 2.25
VDD$_L$=1.62 / 1.62 / 1.98
hysteresis rise
hysteresis fall
SS
TT
FF
2.75 / 2.75 / 2.25
1.62 / 1.98 / 1.98
2.75 / 2.5 / 2.25
1.62 / 1.8 / 1.98
max - min / ns
CORNER
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
1
2
3
4
5
6
7
8
9

FIG. 13D

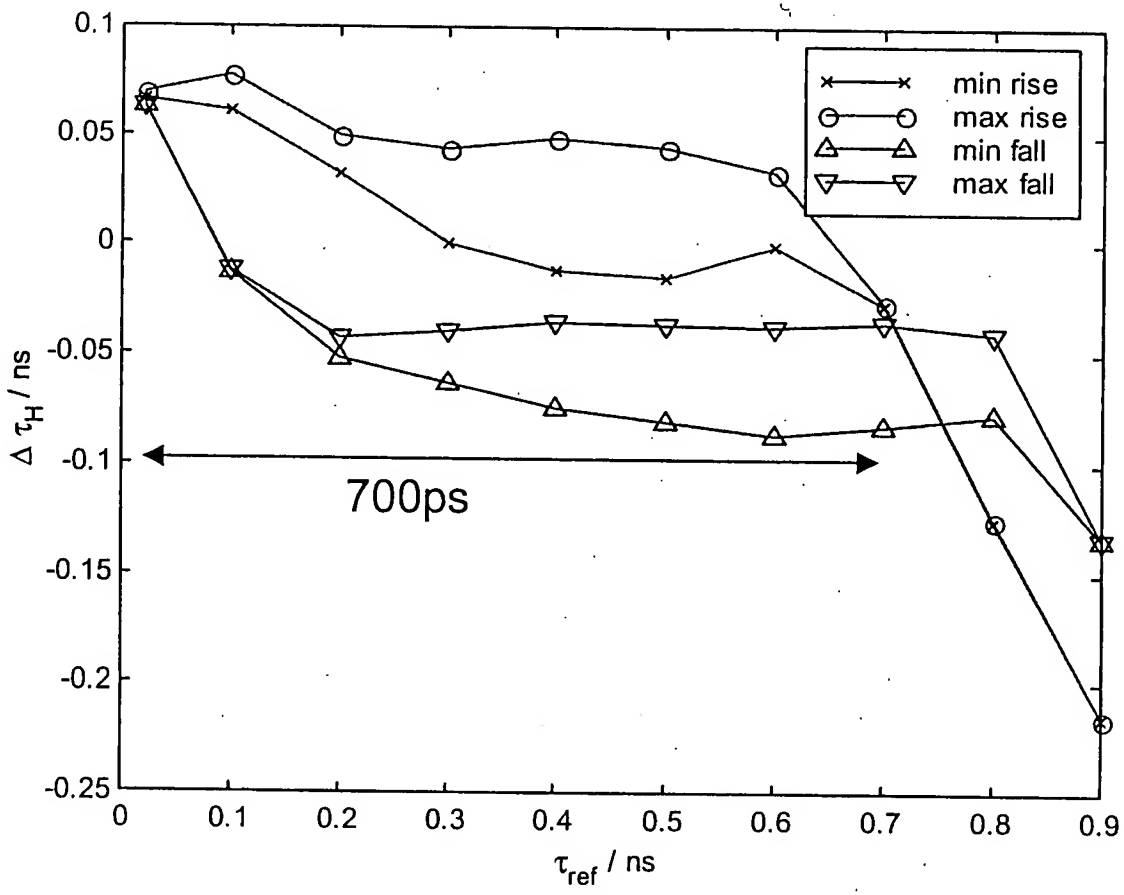
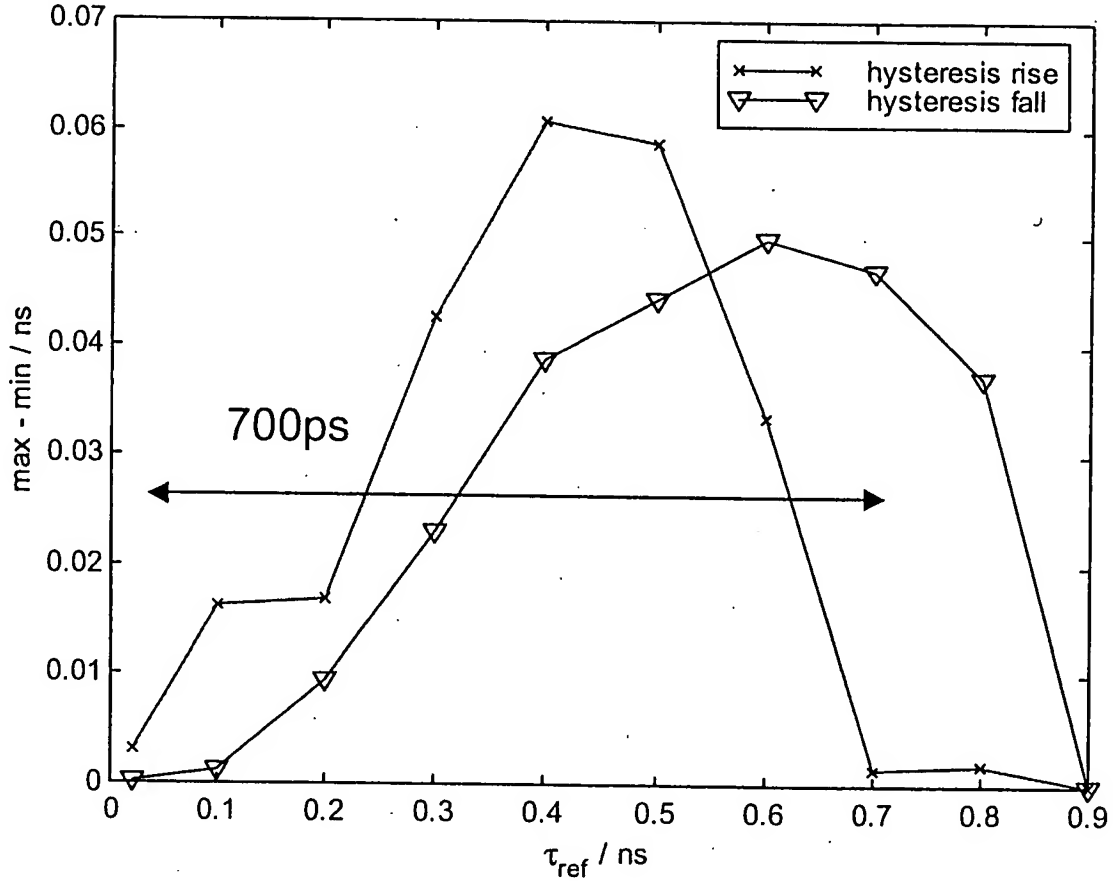

0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
-0.25
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Δ τH / ns
τref / ns
min rise
max rise
min fall
max fall
700ps

FIG. 13E


hysteresis rise
hysteresis fall
700ps
max - min / ns
τ_{ref} / ns
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

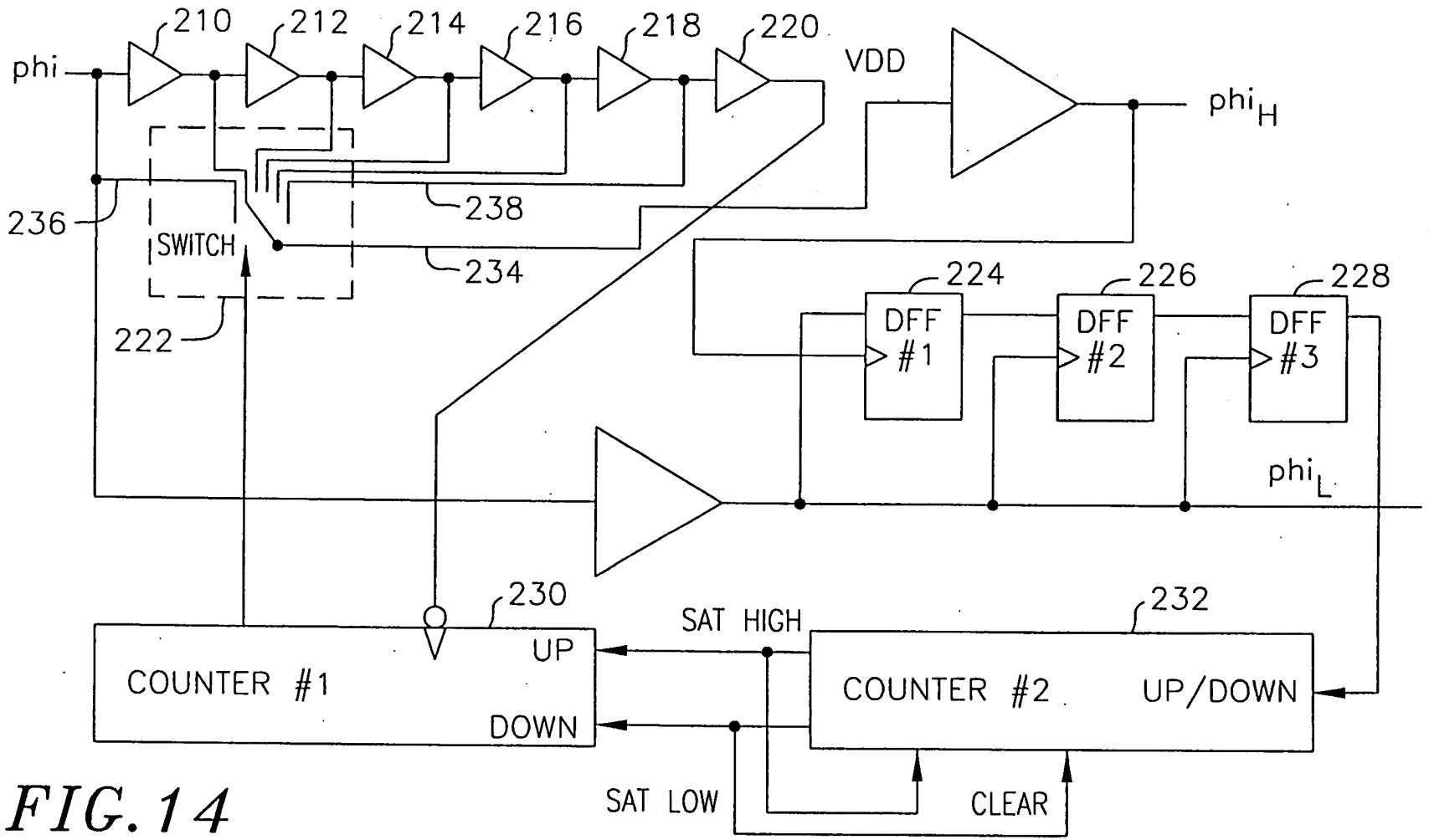

phi
210
212
214
216
218
220
VDD
phi_H
236
238
SWITCH
234
222
224
226
228
DFF #1
DFF #2
DFF #3
phi_L
230
232
SAT HIGH
UP
COUNTER #1
COUNTER #2
UP/DOWN
DOWN
SAT LOW
CLEAR

FIG. 14

FIG. 15

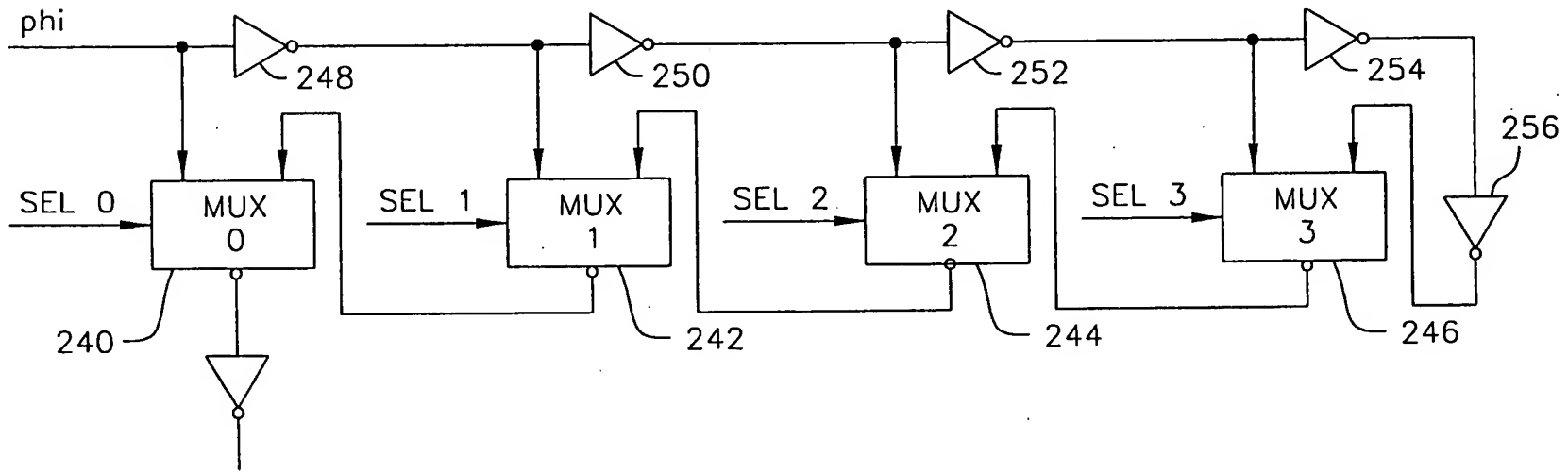
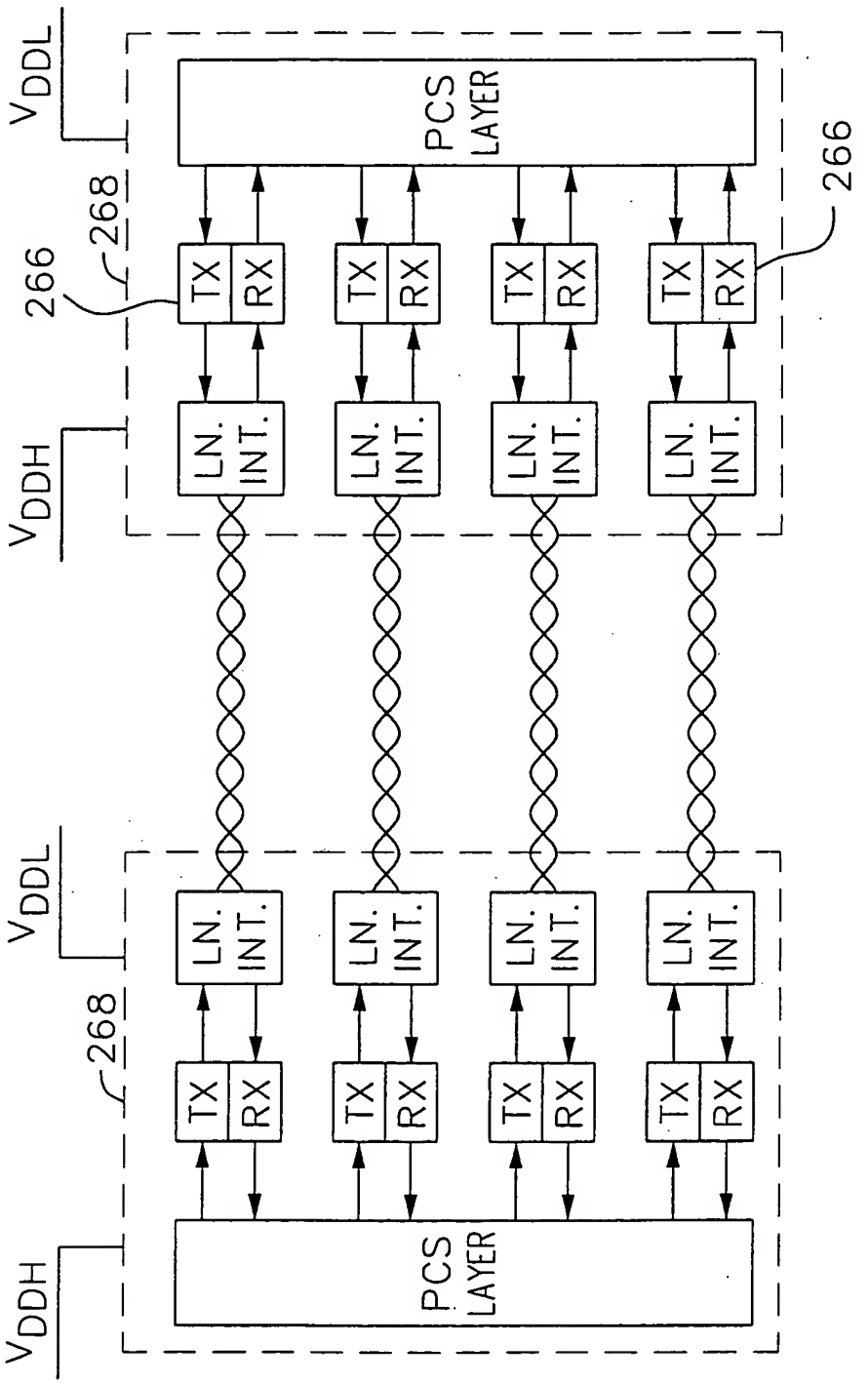

phi
248
250
252
254
256
SEL 0
MUX 0
SEL 1
MUX 1
SEL 2
MUX 2
SEL 3
MUX 3
240
242
244
246

FIG. 16


V_{DDL}
PCS LAYER
266
268
TX
RX
V_{DDH}
LN. INT.
V_{DDL}
268
LN. INT.
TX
RX
V_{DDH}
PCS LAYER

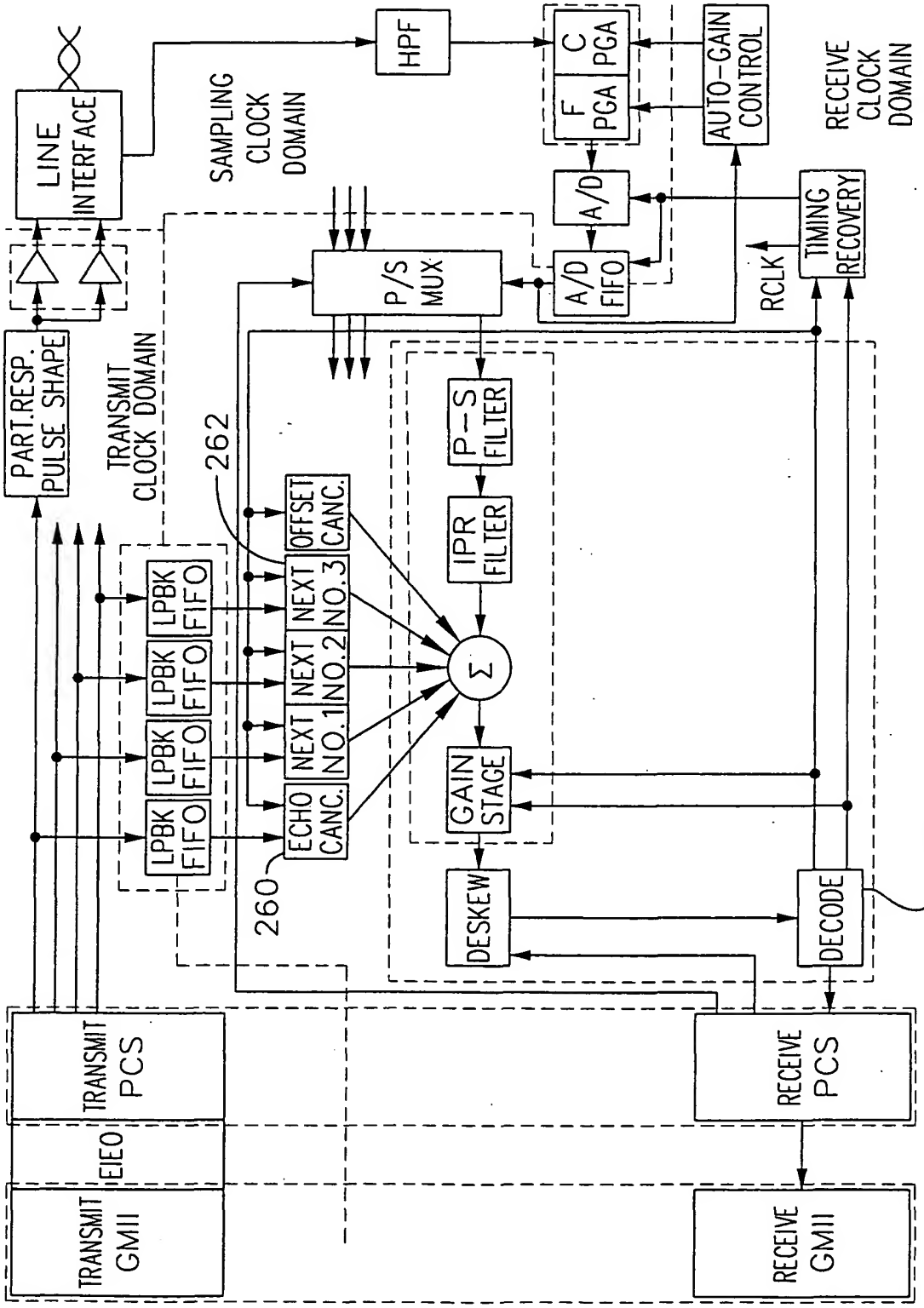
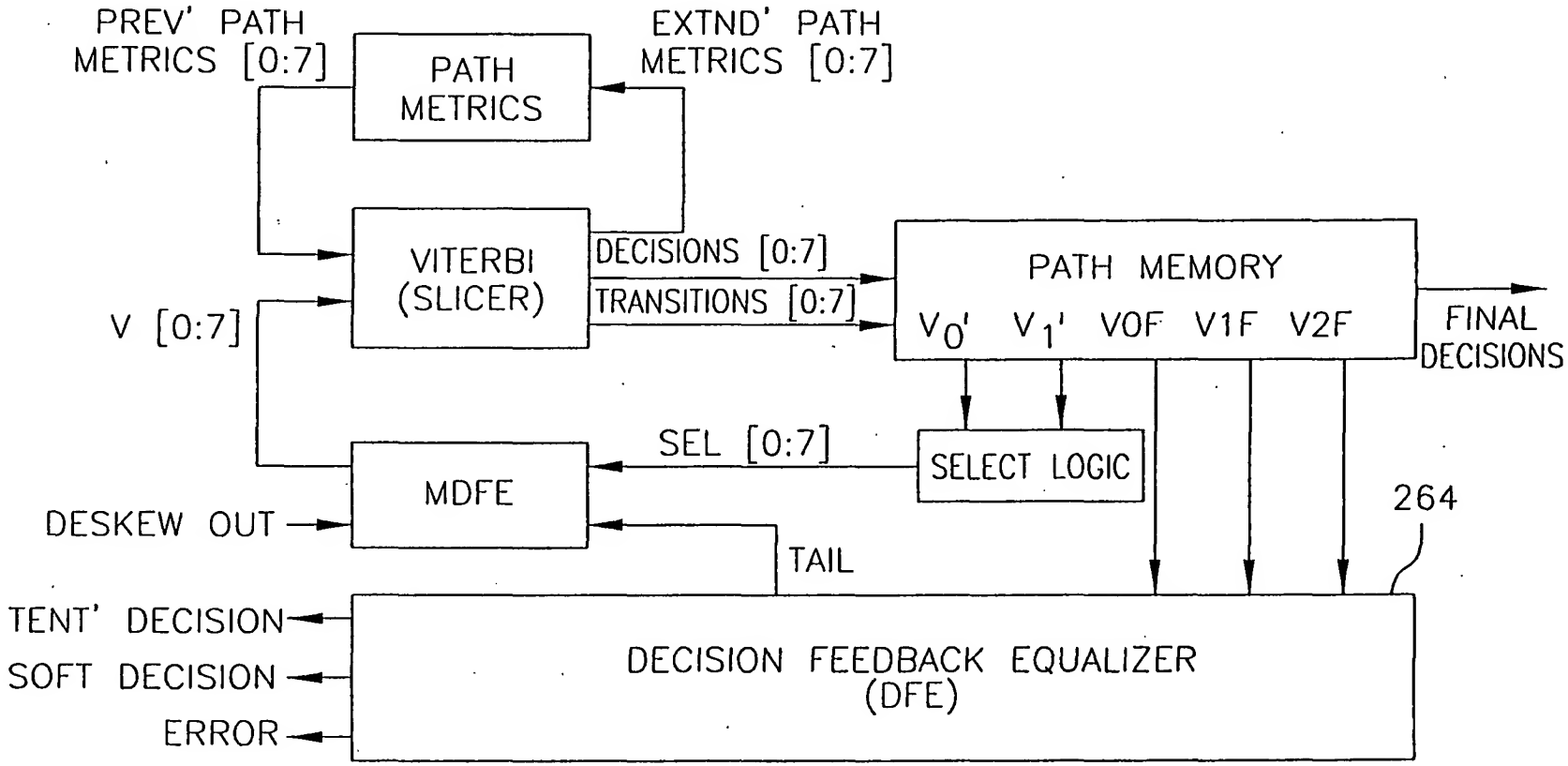

TRANSMIT GMII
EIEO
TRANSMIT PCS
RECEIVE GMII
RECEIVE PCS
TRANSMIT CLOCK DOMAIN
SAMPLING CLOCK DOMAIN
RECEIVE CLOCK DOMAIN
LINE INTERFACE
PART.RESP. PULSE SHAPE
HPF
F PGA
C PGA
AUTO-GAIN CONTROL
A/D
A/D FIFO
P/S MUX
TIMING RECOVERY
RCLK
262
260
270
LPBK FIFO
ECHO CANC.
NEXT NO.1
NEXT NO.2
NEXT NO.3
OFFSET CANC.
Σ
P-S FILTER
IPR FILTER
GAIN STAGE
DESKEW
DECODE

FIG. 17

FIG. 18


PREV' PATH METRICS [0:7]
PATH METRICS
EXTND' PATH METRICS [0:7]
VITERBI (SLICER)
DECISIONS [0:7]
TRANSITIONS [0:7]
PATH MEMORY
V0' V1' V0F V1F V2F
FINAL DECISIONS
V [0:7]
SEL [0:7]
SELECT LOGIC
MDFE
DESKEW OUT
TAIL
264
TENT' DECISION
SOFT DECISION
ERROR
DECISION FEEDBACK EQUALIZER (DFE)